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EXAMINER	
SHAH, CHIRAG G	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,941	HONDA, MASAHIKO	
	Examiner	Art Unit	
	Chirag G. Shah	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/3/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 April 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 have been considered but are moot in view of the new ground(s) of rejection for claim 1. A new non-statutory double patenting rejection with respect to claim 1 has been made in this action.

2. Referring to claims 1, 5, 10, and 14, Applicant argues that Matsumura does not disclose a single controller for controlling the two switch system, nor does Matsumura disclose one of its two control units operating independently of, not communicating with, the second control unit. Examiner respectfully disagrees for at least two reasons. The first reason is in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a single controller for operating independently of, not communicating with, the second control unit) are not recited in the rejected claim(s) 1, 5, 10 and 14. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The second reason is the way the claims 1, 5, 10 and 14 are written with respect to the single controller, the one of two controllers in Matsumura reference still read on the limitation for example, see col. 8, lines 12-20 in Matsumura's reference. Matsumura clearly discloses of a system-switching controller for detecting cell information including delay priority stored in each temporary cell storage unit, for instructing one of temporary cell storage units storing a cell having the highest delay priority among both of active and stand-by systems to read out the cell and for outputting the read out cell form one of

temporary cell storage units selectively to the output selector. Therefore, based on the above reasons claims 1-14 remain rejected under 35 U.S.C. 102(e) as being anticipated by Matsumura et al (U.S. Patent No. 6,269,077).

3. Claims 1, 5, 10, and 14 objected to because of the informalities stated in the office action mailed on 3/8/05 are accepted and therefore the respective objections are withdrawn by the Examiner.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claim 1 rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,269,077. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the present application reads on claim 2 of U.S. Patent No. 6,269,077 when N equals to 1 input selectors. Therefore, it would have been obvious to one skilled in the art at the time of the invention that when N equals to 1 input selectors in the current application, Matsumura claim 2 produces the same expected results.

6. The comparison of the two applications:

Regarding claim 1, a redundant system having two switch routes **[see claim 2, lines 1-3, U.S. Patent No. 6269077]**, comprising:

N, with N greater than or equal to one, input selectors **[N=1 input selector, see claim 2, lines 4]**,

N input lines **[N=1 input line, see claim 2]**,

wherein each N input selector selects one of two switch routes to connect N input lines to selected one of two switch routes, depending on a system switching signal **[see claim 2, lines 4-5, N input selector select the system currently being operated]**;

wherein, two switch sections are provided, one for each one of the two switch routes, each of the two switch sections having N input ports and N output ports, and comprising N buffers **[a temporary cell storage unit is each active and stand-by system, see claim 2, lines 8-11]**,

wherein each of the N buffers comprises M with M greater than or equal to two, priority queues for storing input packets, received from N input selectors, classified under M priorities, and M priority output queues corresponding to the M priorities [see claim 2, lines **[see claim 2, lines 8-15 for temporary cell storage units for receiving and storing delay priority in temporary storage units received from an input selector classified with a delay priority]**;

an output selector for selecting a one of two M priority queue in a one of two switch sections for each of the M priorities to store an output of the selected one of two M priorities queues in a one of two switch sections into a corresponding one of the M

priority output queues **[see claim 2, lines 6-7 and 12-20 for selecting a system currently being operated for selecting the highest delay priority]**; and

a controller for instructing the output selector to select a one of the two priority queues for each of the M priorities corresponding to respective ones of the two switch sections depending on the system switching signal and a packet storing status of each of the M priority queues **[see claims 2, lines 12-20 and 6-7, a control means for instructing one of temporary cell storage units having the highest delay priority to read out the cell and for outputting the read out cell from one of temporary cell storage to the output selector].**

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 rejected under 35 U.S.C. 102(e) as being anticipated by Matsumura et al (U.S. Patent No. 6,269,077), hereinafter, Matsumura.

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the

inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Matsumura discloses a redundant system having two switch routes [see claim 2, lines 1-3, U.S. Patent No. 6269077], comprising:

N, with N greater than or equal to one, input selectors [N=1 input selector, see claim 2, lines 4 and fig. 1],

N input lines [N=1 input line, see claim 2 and fig. 1],

wherein each N input selector selects one of two switch routes to connect N input lines to selected one of two switch routes, depending on a system switching signal [see claim 2, lines 4-5 and fig. 1, N input selector select the system currently being operated];

wherein, two switch sections are provided, one for each one of the two switch routes, each of the two switch sections having N input ports and N output ports, and comprising N buffers [a temporary cell storage unit is each active and stand-by system, see claim 2, lines 8-11 and see fig. 1 and 2],

wherein each of the N buffers comprises M with M greater than or equal to two, priority queues for storing input packets, received from N input selectors, classified under M priorities, and M priority output queues corresponding to the M priorities [see claim 2, lines [see claim 2, lines 8-15 and fig. 2 for temporary cell storage units for receiving and storing delay priority in temporary storage units received from an input selector classified with a delay priority];

an output selector for selecting a one of two M priority queue in a one of two switch sections for each of the M priorities to store an output of the selected one of two M priorities queues in a one of two switch sections into a corresponding one of the M priority output queues [see claim 2, lines 6-7 and 12-20 and fig. 1 for selecting a system currently being operated for selecting the highest delay priority]; and

a controller for instructing the output selector to select a one of the two priority queues for each of the M priorities corresponding to respective ones of the two switch sections depending on the system switching signal and a packet storing status of each of the M priority queues [see claims 2, lines 12-20 and 6-7 and col. 5, liens 35-46, and fig. 1, a control means for instructing one of temporary cell storage units having the highest delay priority to read out the cell and for outputting the read out cell from one of temporary cell storage to the output selector and means for arbitrating cell reading from which temporary cell storage unit is to be performed depending on the cell storage condition].

Regarding claim 5, Matsumura discloses in fig. 1 of a packet switching system having two switch routes, comprising:

N, with N greater than or equal to one, input selectors [for N=1, Input selector 10, see fig. 1], each of which selects a one of two switch routes to connect N lines to the selected one depending on a system switching signal [the input selector selects the active system based on the incoming cell flow signal, see fig. 1 and col. 4, lines 40-50];

two switch sections [active and stand-by systems, see fig. 1], one provided for each of the two switch routes, each of the two switch sections having N input ports and N output ports and comprising N buffers [each system includes input port and output port and temporary cell storage (buffer) unit, see fig. 1], each of which comprises:

a high-priority queue for storing input packets having a high priority, received from N input selectors [each temporary storage unit includes Delay priority m queue, where m>n see fig. 2; the high priority queue receives data from input selector 10, see fig. 1]; and

a low-priority queue for storing input packets having a low priority, received from one of N input selectors [each temporary storage unit includes Delay priority N queue, where m>n see fig. 2; the low priority queue receives data from input selector 10, see fig. 1];

a high-priority output selector for selecting a one of two high-priority queues corresponding to respective ones of the two switch sections [Delay Priority Selector 40 and 50, see fig. 2];

a low-priority output selector for selecting a one of two low-priority queues corresponding to respective ones of the two switch sections [Delay Priority Selector 40 and 50, see fig. 2];

a high priority output queue for storing an output of the selected one of the two high-priority queues [output selector for delivery of cells by selecting one high-priority queues of a system; output selector inherently includes a queues for storing the selected units, see fig. 1 and col. 5, lines 46-66];

a low-priority output queue for storing an output of the selected one of two low-priority queues [output selector for delivery of cells by selecting one low-priority queues of a system;

output selector inherently includes a queues for storing the selected units, see fig. 1 and col. 5, lines 46-66];; and

a controller controlling the high-priority output selectors and the low-priority output selectors of the two switch sections depending on the system switching signal and a packet storing status of each of the high-priority queue and the low priority queues [system switching control unit 21 controls the delay priority selectors of the switch section based on the selected active system and selects, delivers and stores the cells from the delay priority m or n queue to the output selector; controller 21 communicates with other controller 31 to manage the temporary cell storage units 20 and 30 and includes a means for detecting cell information including delay priority stored and means for arbitrating cell reading from which temporary cell storage unit is to be performed depending on the cell storage condition, see fig. 1,2, col. 5, lines 26-46, 57-67 and claim 2].

Regarding claim 10, Matsumura discloses in fig. 1 of a packet switching method in a packet switch having two switch routes and comprising:

N, with N greater than or equal to one, input selectors [for N=1, Input selector 10, see fig. 1], each of which selects a one of two switch routes to connect N lines to the selected switch route depending on a system switching signal [the input selector selects the active system based on the incoming cell flow signal, see fig. 1 and col. 4, lines 40-50];

two switch sections [active and stand-by systems, see fig. 1], one provided for each of the two switch routes, each of the two switch sections having N input ports and N output ports and comprising N buffers [each system includes input port and output port and temporary cell storage

(buffer) unit, see fig. 1], M, with M greater than or equal to two, priority output queues corresponding to respective ones of the M priorities [two delay priority queues corresponding to delay priority M and N see fig. 2]; and

a controller [system-switching controller 21, fig. 1] for selecting a one of two priority queues [see, col. 5, lines 30-52];

the method comprising the steps of:

a) distributing input packets [see fig. 1 and col. 5, lines 4-16], received from N input selectors [input selector 10, see fig. 1], into M priority queues [see fig. 2, delay priority queue m and n], which are classified under M priorities for each of the N buffers [temporary cell storage unit 20 with m and n priorities, see fig. 2]; and

b) selecting, by a single controller, one of two priority queues for each of the M priorities corresponding to respective ones of the two switch sections to store an output of the selected one of two priority queues into a corresponding one of the M priority output queues, depending on a system switching signal and a packet storing status of each of the M priority queues [system switching control unit 21 controls the delay priority selectors of the switch section based on the selected active system and selects, delivers and stores the cells from the delay priority m or n queue to the output selector; controller 21 communicates with other controller 31 to manage the temporary cell storage units 20 and 30 and includes a means for detecting cell information including delay priority stored and means for arbitrating cell reading from which temporary cell storage unit is to be performed depending on the cell storage condition, see fig. 1,2, col. 5, lines 26-45, 57-67 and claim 2].

Regarding claim 14, Matsumura discloses in fig. 1 of a method for controlling a packet switch having two switch routes and comprising:

N, with N greater than or equal to one, input selectors [for N=1, Input selector 10, see fig. 1], each of which selects a one of two switch routes to connect N lines to the selected switch route depending on a system switching signal [the input selector selects the active system based on the incoming cell flow signal, see fig. 1 and col. 4, lines 40-50];

two switch sections [active and stand-by systems, see fig. 1], one provided for each of the two switch routes, each of the two switch sections having N input ports and N output ports and comprising N buffers [each system includes input port and output port and temporary cell storage (buffer) unit, see fig. 1], M, with M greater than or equal to two, priority output queues corresponding to respective ones of the M priorities [tow delay priority queues corresponding to delay priority M and N see fig. 2]; and

a controller [system-switching controller 21, fig. 1] for switching the two switch section [see, col. 5, lines 30-52];

the method comprising the steps of:

a) distributing input packets [see fig. 1 and col. 5, lines 4-16], received from N input selectors [input selector 10, see fig. 1], into M priority queues [see fig. 2, delay priority queue m and n], which are classified under M priorities for each of the N buffers [temporary cell storage unit 20 with m and n priorities, see fig. 2]; and

b) sequentially switching, by a single controller [the delay priority selector performs selective operation in accordance with the control of the system-switching controller 21 or 31 and enables simultaneous control of the temporary cells unit of active and standby system so that

cells in them can be read out in the order of their delay priority, see col. 5, lines 46-66 and col. 6, liens 14-19],

one of two priority queues for each of the M priorities corresponding to respective ones of the two switch sections to store an output of the selected one of two priority queues into a corresponding one of the M priority output queues, depending on a system switching signal and a packet storing status of each of the M priority queues in descending as order of priority [the system-switching control instructs the output selector to read out cells from the temporary cell storage unit in the order of higher delay priority; system switching control unit 21 controls the delay priority selectors of the switch section based on the selected active system and selects, delivers and stores the cells from the delay priority m or n queue to the output selector; controller 21 communicates with other controller 31 to manage the temporary cell storage units 20 and 30 and includes a means for detecting cell information including delay priority stored and means for arbitrating cell reading from which temporary cell storage unit is to be performed depending on the cell storage condition, see fig. 1,2, col. 5, lines 4-16, 26-45, 57-67 and claim 2].

Regarding claim 2, wherein when the one of the two switch routes is switched to an other switch route by the system switching signal [system switching control means comprises a system-switching control units as disclosed in col. 2, lines 32-65], the controller monitors a packet storing status of each of the high-priority and low-priority queues [system-switching control unit 21 or 31, in each system mutually communicates with each other and manages a temporary cell storage nit, in which cells to be read out are stored in accordance with the delay priority group as disclosed in figure 1 and abstract] and, if the one of the two high-priority

queues corresponding to respective ones of the two switch sections becomes empty, then the controller instructs the high-priority output selector to select the other of the two high-priority queues to store an output of the selected one of two M priority queues (the high-priority output queue) in a one of two switch sections into the high-priority output queue [as disclosed in column 2, lines 18-48, column 4, lines 57-59, column 5, lines 35-46, control means for arbitrating cell reading form which temporary cell storage unit is to be performed depending on cell storage condition] as claims.

Regarding claim 3, Matsumura discloses that the switch section further comprises a readout controller [read control unit 204 in figure 3] controlling a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that priority in packet reading is given to the high-priority queue [as disclosed in figure 1, 3 and in column 5, lines 4-16, the system-switching control unit 21 instructs to the temporary cell storage unit 20 to read out cells in the order of higher delay priority. Thus cells are read out successively in he order of their delay priorities] as claims.

Regarding claim 4, Matsumura discloses wherein the controller instructs the output selector to sequentially select the other of the two priority queues for each of the M priorities in descending order of priority [as disclosed in column 5, lines 4-16, 35-52 that the system-switching control instructs the output selector to read out cells from the temporary cell storage unit in the order of higher delay priority] as claim.

Regarding claim 6, wherein when the one of the two switch routes is switched to an other switch route by the system switching signal [system switching control means comprises a system-switching control units as disclosed in col. 2, lines 32-65], the controller monitors a packet storing status of each of the high-priority and low-priority queues [system-switching control unit 21 or 31, in each system mutually communicates with each other and manages a temporary cell storage nit, in which cells to be read out are stored in accordance with the delay priority group as disclosed in figure 1 and abstract] and, if the one of the two high-priority queues corresponding to respective ones of the two switch sections becomes empty, then the controller instructs the high-priority output selector to select the other of the two high-priority queues to store an output of the selected one of two M priority queues (the high-priority output queue) in a one of two switch sections into the high-priority output queue [as disclosed in column 2, lines 18-48, column 4, lines 57-59, column 5, lines 35-46, control means for arbitrating cell reading form which temporary cell storage unit is to be performed depending on cell storage condition] as claims.

Regarding claim 7, Matsumura discloses that the switch section further comprises a readout controller [read control unit 204 in figure 3] controlling a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that priority in packet reading is given to the high-priority queue [as disclosed in figure 1, 3 and in column 5, lines 4-16, the system-switching control unit 21 instructs to the temporary cell storage unit 20 to read out cells in the order of higher delay priority. Thus cells are read out successively in he order of their delay priorities] as claims.

Regarding claim 8, Matsumura discloses wherein the readout controller starts reading out low-priority packet stored in the low-priority queue after all high-priority packets stored in the high priority queue have been completely read out [as disclosed in column 5, lines 4-16 and in column 6, lines 57-64, once all cells in the same priority group (high priority) have been read out, then cells in the next priority order group are to be read out] as claim.

Regarding claim 9, Matsumura discloses wherein the readout controller controls a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that m high-priority packets are read out from the higher-priority queue and n low-priority packets are read out from the low-priority queue, wherein m is set to be greater than n [see, column 5, liens 4-16, fig. 2 and claim 2].

Regarding claim 11, Matsumura discloses wherein when the one of the two switch routes is switched to an other switch route by the system switching signal [system switching control means comprises a system-switching control units as disclosed in col. 2, lines 32-65], the controller monitors a packet storing status of each of the high-priority and low-priority queues [system-switching control unit 21 or 31, in each system mutually communicates with each other and manages a temporary cell storage nit, in which cells to be read out are stored in accordance with the delay priority group as disclosed in figure 1 and abstract] and, if the one of the two high-priority queues corresponding to respective ones of the two switch sections becomes empty, then the controller instructs the high-priority output selector to select the other of the two high-priority

queues to store an output of the selected one of two M priority queues (the high-priority output queue) in a one of two switch sections into the high-priority output queue [as disclosed in column 2, lines 18-48, column 4, lines 57-59, column 5, lines 35-46, control means for arbitrating cell reading form which temporary cell storage unit is to be performed depending on cell storage condition] as claims.

Regarding claim 12, Matsumura discloses that the switch section further comprises a readout controller [read control unit 204 in figure 3] controlling a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that priority in packet reading is given to the high-priority queue [as disclosed in figure 1, 3 and in column 5, lines 4-16, the system-switching control unit 21 instructs to the temporary cell storage unit 20 to read out cells in the order of higher delay priority. Thus cells are read out successively in he order of their delay priorities] as claims.

Regarding claim 13, Matsumura discloses wherein the controller instructs the output selector to sequentially select the other of the two priority queues for each of the M priorities in descending order of priority [as disclosed in column 5, lines 4-16, 35-52 that the system-switching control instructs the output selector to read out cells from the temporary cell storage unit in the order of higher delay priority] as claim.

Conclusion

Any response to this action should be faxed to:

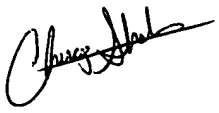
(571)272-8300, (for formal communications intended for entry)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs
August 23, 2005



Chirag Shah